InEW 2025
India ESD Workshop

IEEE Advancing Technology for Humanity

FREE TUTORIAL @

25th - 26th August 2025

6th India ESD Workshop

Indian Institute of Science, Bangalore, India

Mode: Online
Start Date: August 11th
Eligibility: Available only to those who register for the 6th India ESD Workshop

Tutorial on On-Chip ESD Device & Circuit Design

Designing on-chip ESD protection devices and circuits is a highly specialized field. While this knowledge is accessible through academic research and industry forums, it remains niche and is often shared within limited circles of experts. Many engineers and professionals, even those with some exposure to ESD-related domains, may not have direct experience with ESD device physics or circuit design methodologies.

Over the years, participants of the India ESD Workshop (InEW) have consistently expressed that while the workshop offers advanced, in-depth technical content, those without a strong foundation in ESD often find it challenging to follow. Recognizing this gap, we have received repeated requests to offer introductory material that can help participants build the necessary foundational knowledge before attending the workshop.

In response to this valuable feedback and with over a thousand participants having benefited from InEW over the years, we are excited to announce that free online tutorial sessions will be offered two weeks prior to the start of the 6th India ESD Workshop (InEW). These tutorials are designed to cover the basics of ESD device physics and circuit design, enabling all registered participants to better engage with and benefit from the advanced content presented during the main event.

Eligibility: All individuals registered for the 6th InEW will receive access to these live online tutorials.

We believe this initiative will significantly enhance the learning experience and help foster a broader and more inclusive ESD design community.

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1) Fundamentals of ESD and ESD Design – 4 Hrs

- Introduction to EOS/ESD and Factory measures
- Test standards (HBM, CDM, MM)
- TLP for Device Modeling and Characterization
- ESD Design Window
- ESD Consequences and Simplified ESD Protection Strategy
- ESD Protection with Ground Separation and Multiple Power Rails
- ESD protection for Digital I/Os, Rail Based ESD and Local Clamp Protection, Inter/Intra Domain ESD Stress, b/w Power Rails, Package level Protection Measures, System in Package

2) High Current Device Physics Under ESD Condition – 6 Hrs

- Basic ESD Devices – (1) Resistor, (2) Diode, (3) SCR and (4) ggNMOS
- Advanced ESD Devices – (1) BJT and (2) DeMOS/LDMOS

3) ESD Protection Circuit Design Concepts and Strategy – 4 Hrs

- Qualities of Good ESD Protection
- RCMOS Based Power Clamp Design
- ESD Protection Design Methods – (1) Local Clamps and (2) Rail-to-Rail Clamps
- Diode Based Clamps, ggNMOS Based Clamps, SCR Based Clamps, Fail Safe Protection, HV ESD protection, p-DeMOS Based Clamps
- Secondary Protection Design
- Other Considerations

Click on link to Register: ***https://iisc-inew2025.registeryourseat.in/***

Venue: Indian Institute of Science, Bangalore
Organized By: Prof. Mayank Shrivastava (IISc)

Web: https://iisc-inew.org/
E-mail: Indiaesdworkshop@gmail.com