InEW 2025
India ESD Workshop

IEEE
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25th - 26th August 2025

6th India ESD Workshop

Indian Institute of Science, Bangalore, India

TECHNICAL PROGRAM

Venue: Indian Institute of Science, Bangalore
Organised By: Prof. Mayank Shrivastava (IISc)

Web: https://iisc-inew.org/
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InEW 2025 India ESD Workshop

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About the India ESD Workshop (InEW)

ESD reliability understanding and how to design ESD safe chips have always been highly important and crucial aspects for semiconductor design, development, testing, and manufacturing cycles. Given the absence of ESD design/testing/technology knowledge, expertise, and awareness in India, in 2015 **Indian Institute of Science (IISc), Bangalore** started efforts for industry professionals and students, which today is called **India ESD Workshop (InEW).** This conference has gathered significant interest and traction from the semiconductor industry professionals in India, with the potential to expand to other regions going forward. For example, the last edition attracted 250+ senior-level engineers from the semiconductor industry. The conference has also flourished due to its significant collaborations with industry leaders like Intel, Samsung, Texas Instruments, Western Digital, Global Foundry, Qualcomm, Synopsys, Cadence and NXP etc. The objective of the conference has always been to promote the knowledge, know-how, and expertise in ESD design, technology, and testing, in collaboration with global ESD experts. With the growing manufacturing requirements, manufacturing push in the country, upcoming fabs, an increasing number of chip design centers getting into full product cycles (full product developments), and an increasing number of chip design start-ups with efforts on end products, this expertise becomes more than relevant and justifies the need and growth of venues like InEW to continue and grow. With the current context, it would not be an exaggeration if the conference grows to 500+ professionals in the years to come.

Poster Session

An interactive Poster Session of 30 plus posters with High Tea. Participants get to see a variety of world class research done in the area of Electrostatic discharge and get to ask questions and engage in dialogue with the presenters.

Meet World Renowned Experts

A platform for poised to revolutionize the way industry leaders connect with top-tier talent. Our platform ensures that every expert in the field of Electrostatic Discharge is showcased to potential collaborators and employers on a global scale.

Industry Sessions

Heated and seated discussion sessions, in a relaxed setting, on emerging technological areas or key showstoppers or major scientific debates with a quest to find the role academia must play in the next 10 years.

Panel Discussion

To brainstorm on the major ESD induced bottlenecks in the cutting edge technologies and products in the Semiconductor Industry.

Industry Interaction

Conducting collaborative brainstorming sessions to explore opportunities for closer engagement with the industry. This initiative aims to establish a distinctive platform for fostering robust academia-industry partnerships, culminating in the development of a comprehensive 10-year plan and roadmap.

Young Researchers Meet

A special session to explore research opportunities in leading R&D Labs and academic institutions in India.

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Workshop Highlights

03	Keynote Talks	01	Panel Session
30+	Technical Talks	13	Platform Presentations
30+	Poster Presentations	250+	Attendees

Why Attend and Participate?

- Global Engagement: Collaborate with international ESD design experts, resolving design complexities and pioneering resilient ESD design and protection strategies.
- Cutting-edge Discoveries: Dive deep into innovative process technologies, gaining insights into their global implications and applications.
- Expansive Networking: Connect with global peers, industry leaders, and academics, establishing valuable partnerships for the future.
- Present and Propel: Showcase your work on a global stage, attracting diverse perspectives, accolades, and potentially setting industry standards.
- For Students: A unique platform to learn, shine, and perhaps, chart a future course with potential employers from across the globe.
- Relevance to the Global Community: At a time when electronic intricacies intersect with the demand for robustness and reliability, understanding ESD challenges is not just essential; it's critical. InEW-2025 promises to be the crucible where knowledge meets application, innovation meets industry, and challenges meet solutions. It aims to not only address current ESD challenges but also proactively envision and counter future hurdles, ensuring the global VLSI community stays ahead of the curve.

As we stand on the cusp of technological revolutions, with semiconductor technologies reaching their fundamental limits, and devices becoming smarter and more interconnected, the significance of ESD reliability cannot be overstated. Join us at India ESD Workshop 2025. Be part of this global movement, shaping the trajectory of On-Chip and System level ESD design and reliability physics in the realm of a plethora of semiconductor technologies. Together, let's drive a global ESD knowledge renaissance for a technologically resilient future.

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Topics of Interest

1. Advanced CMOS: FinFET, Nanowires, Nanosheets, etc.

ESD Issues in Advanced Technologies (Multi-gate, FinFET, SOI, SiGe, nanowire, etc.), On-Chip ESD Protection Devices & Techniques in Advanced CMOS Technologies, IC Design and Layout Issues, Circuit Simulation of EOS/ESD Events in Advanced CMOS Technologies, DC/Transient Latch-up Issues and Solutions.

2. Emerging Technologies: 2D, RRAM, Neuromorphic Devices, Quantum, etc.

ESD issues in novel devices with 2D layered semiconductor or dielectric materials, logic and memory devices, neuromorphic devices, quantum devices and quantum enhanced technologies.

3. 2.5D & 3D Stacking, TSV, Backside Power Delivery Network

ESD Issues and solutions in 2.5D & 3D IC packaging and integration, interconnects, TSV, ESD protection requirements in Backside Power Delivery Network.

4. Analog & Automotive Technologies: Bipolar, RF, High Voltage, and BCD

ESD Issues, on-chip ESD protection devices and techniques, IC Design and layout issues, ESD circuit simulation and co-design, DC/Transient Latch-up Issues and Solutions in Bipolar, RF, High Voltage, and BCD Technologies.

5. ESD Testing

ESD Testing trends with Technology Scaling, Multi-dimensional packaging, ESD Test and Characterization method, Traditional and Novel TLP Testing System, HBM and CDM testing issues and solutions, Reliability Test equipment,New failure mechanism, Advance failure analysis techniques, ESD Checking and verification Technology.

6. ESD Device & System Modelling

System level Test, modeling and simulation method, Circuit level design and simulation of ESD Events in Advanced CMOS Technologies, Use of EDA tools, IC Design and Layout issues, Transient ESD induced upset, Robustness evaluation for standard test boards,Large scale analysis with machine and deep learning.

7. Numerical Modeling and Simulation of ESD Components

Component level ESD design including but not limited to SCR, LDMOS, GGNMOS, GDPMOS, Diode, etc., TCAD/Circuit Simulation, Numerical modeling and Physics od ESD events, Advance simulation technologies (SOI, SiGe, FinFET, Compound, Nanowire),Latchup detection prevention and mitigation, Simulation tools and methodology.

8. ESD CAD & Verification

ESD modeling, design guidelines, testing standards, whole chip ESD protection, design verification, compliance testing, ESD Protection for mixed voltage applications.

9. System Level ESD

System efficient ESD design (SEED), ESD testing standards (IEC), co-design methodology of on-board and on-chip ESD protection, ESD protection for consumer electronics, automotive, aerospace and industrial applications, Advancements in System level IEC qualification test methods like Air-discharge tests, Development challenges related to off-chip protection elements with ultra-low capacitances.

10. ESD and EOS Protection in GaN HEMTs & GaN Power ICs

GaN technology based ESD protection diodes, TVS, testing and shielding techniques, EOS protection from overvoltage conditions, current surges and power supply instability.

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Key Dates

June 25th	Poster Submission
June 30th	Poster Acceptance
June 30th	Program Announcement
August 15th	Early Bird Registration Deadline
August 21st	Late Registration Deadline
August 25th - 26th	India ESD Workshop

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Pre-Conference Tutorial

Mode: Online

Start Date: August 11th

Eligibility: Available only to those who register for the 6th India ESD Workshop

Tutorial on On-Chip ESD Device & Circuit Design

Designing on-chip ESD protection devices and circuits is a highly specialized field. While this knowledge is accessible through academic research and industry forums, it remains niche and is often shared within limited circles of experts. Many engineers and professionals, even those with some exposure to ESD-related domains, may not have direct experience with ESD device physics or circuit design methodologies. Over the years, participants of the India ESD Workshop (InEW) have consistently expressed that while the workshop offers advanced, in-depth technical content, those without a strong foundation in ESD often find it challenging to follow. Recognizing this gap, we have received repeated requests to offer introductory material that can help participants build the necessary foundational knowledge before attending the workshop. In response to this valuable feedback and with over a thousand participants having benefited from InEW over the years, we are excited to announce that free online tutorial sessions will be offered two weeks prior to the start of the 6th India ESD Workshop (InEW). These tutorials are designed to cover the basics of ESD device physics and circuit design, enabling all registered participants to better engage with and benefit from the advanced content presented during the main event.

Eligibility: All individuals registered for the 6th InEW will receive access to these live online tutorials.

We believe this initiative will significantly enhance the learning experience and help foster a broader and more inclusive ESD design community.

1) Fundamentals of ESD and ESD Design – 4 Hrs

- Introduction to EOS/ESD and Factory measures
- Test standards (HBM, CDM, MM)
- TLP for Device Modeling and Characterization
- ESD Design Window
- ESD Consequences and Simplified ESD Protection Strategy
- ESD Protection with Ground Separation and Multiple Power Rails
- ESD protection for Digital I/Os, Rail Based ESD and Local Clamp Protection, Inter/Intra Domain ESD Stress, b/w Power Rails, Package level Protection Measures, System in Package

2) High Current Device Physics Under ESD Condition – 6 Hrs

- Basic ESD Devices – (1) Resistor, (2) Diode, (3) SCR and (4) ggNMOS
- Advanced ESD Devices – (1) BJT and (2) DeMOS/LDMOS

3) ESD Protection Circuit Design Concepts and Strategy – 4 Hrs

- Qualities of Good ESD Protection
- RCMOS Based Power Clamp Design
- ESD Protection Design Methods – (1) Local Clamps and (2) Rail-to-Rail Clamps
- Diode Based Clamps, ggNMOS Based Clamps, SCR Based Clamps, Fail Safe Protection, HV ESD protection, p-DeMOS Based Clamps
- Secondary Protection Design
- Other Considerations

Click on link to Register: ***https://iisc-inew2025.registeryourseat.in/***

www.iisc-inew.org

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Program Schedule

Day 1 (25th Monday August)

Time	Duration	Speaker & Affiliation	Talk Details
09:30 AM	15 Mins	Welcome and Inaugural Address	
09:45 AM	45 Mins	**Dr. Harald Gossner** (Intel, Germany)	ESD Protection Challenges for AI Compute Applications (Keynote)
10:30 AM	30 Mins	**Dr. Slavica Malobabic** (Cirrus Logic, USA)	Parasitic PNPs and NPNs in ESD and latch up over different time domains (Invited*)
11:00 AM	30 Mins	Break	Break
11:30 AM	30 Mins	**Dr. Efraim Aharoni** (Tower Semiconductor, Israel)	Foundry ESD deliverables and characterization for ESD for ESD (Invited)
12:00 PM	30 Mins	**Mr. Vinayakam Subramanian** (Ansys, India)	2.5D/3D-IC ESD Reliability Analysis (Invited)
12:30 PM	30 Mins	**Prof. Nathan Jack** (Brigham Young University Idaho, USA)	Latchup in Contemporary and Emerging CMOS Technologies (Invited)
01:00 PM	90 Mins	Networking Lunch	Networking Lunch
02:30 PM	30 Mins	**Mr. Matthew Hogan** (Siemens EDA, USA)	Improving the fidelity of ESD margins with context-aware ESD simulation (Invited)
03:00 PM	30 Mins	**Dr. Ann Concannon** (Texas Instruments, USA)	Navigating ESD protection challenges in Analog design (Invited)
03:30 PM	20 Mins	**Mr. Mitesh Goyal** (Indian Institute of Science)	Novel Trigger Circuit & SCR Device Co-Engineering Based Local (I/O-VSS & I/O-VDD) ESD Clamp Concepts (Ph.D. Talk)
03:50 PM	20 Mins	**Mr. Harsh Raj** (Indian Institute of Science)	Dynamic Breakdown Voltage and Overvoltage Margin in beta-Ga2O3 based devices (Ph.D. Talk)
04:10 PM	20 Mins	**Mr. Mayank Yadav** (Indian Institute of Science)	Proposal to Achieve the Ultimate Holding Voltage Tunability in Silicon Controlled Rectifiers (SCRs) for a Wide Range of ESD Protection Application (Ph.D. Talk)
04:30 PM	30 Mins	Coffee Break	Coffee Break
05:00 PM	60 Mins	Panel Moderator: **Prof. Mayank Shrivastava** (Indian Institute of Science)	Panel Session (Growing ESD Challenges in Next Generation Semiconductor Technologies)
06:00 PM	90 Mins	Poster Session	
07:30 PM	120 Mins	Chair's Reception & Dinner	

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Program Schedule

Day 2 (26th Tuesday August)

Time	Duration	Speaker & Affiliation	Talk Details
09:00 AM	45 Mins	**Dr. Wolfgang Stadler** (Intel, Germany)	ESD Control for Chip Designers & Test Engineers (Keynote*)
09:45 AM	40 Mins	**Dr. Charvaka Duvvury** (iT2 Technologies, USA)	Five Decades of ESD Technology Development: Breakthrough Events and Milestones (Keynote)
10:30 AM	10 Mins	**Dr. Stefen Holland** (Nexperia Germany GmbH)	System level ESD protection for high-speed data lines (Invited)
11:00 AM	20 Mins	**Break**	**Break**
11:20 AM	10 Mins	**Dr. Shin-ichi Iida** (ULVAC-PHI)	Advanced Surface and InterfaceCharacterization for Semiconductor Devices Using XPS and SIMS (Platform Presentation*)
11:30 AM	30 Mins	**Prof. Carlo De Santi** (University of Padova, Italy)	TLP effects on normally-off p-GaN gate power HEMTs with Schottky gate (Invited)
12:00 PM	30 Mins	**Mr. Marcos Hernandez** (Thermo Fisher Scientific)	Charge Device Model (CDM) Electrostatic Discharge Test Using Low Impedance Contact CDM Method (LI-CCDM) (Contributed Talk)
12:30 PM	20 Mins	**Dr. Krzysztof Domanski** (Intel Germany)	ESD codesign in leading-edge Ribbon-FET technologies (Invited*)
01:00 PM	90 Mins	**Networking Lunch**	**Networking Lunch**
02:30 PM	30 Mins	**Dr. Karuna Nidhi** (Tata Semiconductor Manufacturing Pvt. Ltd. Taiwan)	ESD Design flow and Major concern for ICs (Invited)
03:00 PM	30 Mins	**Dr. Akram A Salman** (Samsung Electronics, South Korea)	State-of-the-art advances in ESD design & testing for Digital and Analog technologies (Invited)
03:30 PM	30 Mins	**Dr. Ping-Hsun, Su** Tata Semiconductor Manufacturing Pvt. Ltd.Taiwan)	ESD Challenges from Process transfer into different Fabs (Invited)
04:00 PM	30 Mins	**Coffee Break**	**Coffee Break**
04:30 PM	15 Mins	**Prof. Sandip Lashkare** (IIT Gandhinagar)	Design Challenges and Considerations for Low Voltage System Level ESD Protection Devices (Contributed Talk)
04:45 PM	15 Mins	**Mr. Harshit Dhakad** (Intel)	Unraveling ESD HBM Failure on a Failsafe Interface in an Advanced FINFET Technology Node (Contributed Talk)
05:00 PM	15 Mins	**Mr. Surya Viswanathan** (Infineon)	CDM robustness improvement through decoupling capacitors in advanced CMOS technologies (Contributed Talk)

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Program Schedule

Day 2 (26th Tuesday August)

Time	Duration	Speaker & Affiliation	Talk Details
05:15 PM	15 Mins	**Mr. Vinod Kumar** (Cadence Design Systems)	ESD challenges of Designing high-speed interfaces in advanced nodes (Contributed Talk)
05:30 PM	15 Mins	**Mr. Gopikrishna Siddula** (Western Digital)	Designing ESD-Robust ASICs: A Practical Approach for Teams Without ESD Specialists (Contributed Talk)
05:45 PM	15 Mins	**Yogendri Vishwakarma** (Rambus)	Advanced EOS protection techniques (Contributed Talk)
06:00 PM	15 Mins	**Prof. Laxmeesha Somappa** (IIT Bombay)	On the ESD requirements and implementation challenges of Neural SoCs (Contributed Talk)
06:15 PM	15 Mins	**Ms. Roopa Hegde** (Lam Research)	Process window optimization for gate-all-around Electrostatic Discharge (ESD) diode
06:30 PM	15 Mins	**Mr. Yaddanapudi Vamsi Krishna** (Ansys)	Simulation Solutions for Electrostatic Discharge (Platform Presentation)
06:45 PM	10 Mins	**Mr. Tristen Tan** (Rohde & Schwarz)	ESD Transient Pulse Verification Based on Oscilloscope (Platform Presentation)
06:55 PM	10 Mins	**Mr. Sadaf Arif Siddiqui** (Keysight Technologies)	Advancements in Semicon test validation with ESD perspective (Platform Presentation)
07:05 PM	15 Mins	**Concluding Remarks & Vote of Thanks & 7th InEW Announcement**	
07:20 PM	10 Mins	**Networking, Poster, Hi-tea, and See You @ 7th InEW**	

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Panel Discussion

Panel Discussion: Growing ESD Challenges in Next Generation Semiconductor Technologies
Date & Time: August 25, 2025, 5:00 PM - 6:00 PM
Moderator: Prof. Mayank Shrivastava, Indian Institute of Science

Session Overview

The semiconductor industry is undergoing rapid advancements, with new technologies pushing the boundaries of what is possible. However, these advancements also bring about new challenges, particularly in the realm of Electrostatic Discharge (ESD) protection. As semiconductor devices become smaller, faster, and more integrated, the need for robust ESD solutions becomes more critical. This panel session will bring together leading experts from academia and industry to discuss and debate the emerging ESD challenges associated with next-generation semiconductor technologies.

Panellists & Topics

Dr. Harald Josef Erhard Gossner (Intel Corporation, Germany)
Topic: Discussion on the evolution of CMOS nodes over the next 15 years, focusing on advanced and 3D packaging, heterogeneous integration, backside power rails, and the impact of newer materials like 2D materials on ESD design and protection.

Dr. Steffen Holland (Technical Director, Nexperia Germany GmbH)
Topic: Exploration of ESD challenges in advanced automotive nodes, system-level ESD issues in electric vehicles (EVs), and the specific requirements of advanced automotive and EV applications.

Dr. Ann Concannon (DMTS, Texas Instruments)
Topic: Examination of the growing complexity of ESD issues and the role of advanced computational and simulation techniques in addressing these challenges. Emphasis on the need for more sophisticated simulation approaches as semiconductor technologies continue to evolve.

Dr. Akram A Salman (VP/Master Samsung Fondary (ESD team leader) Samsung Electronics,South Korea)
Topic: Insight into the unique ESD challenges posed by next generation and futuristic technologies. Discussion on the critical role that academia plays in addressing scientifically challenging problems that are beyond the current capabilities of industry, and the importance of industry-academia collaborations.

Session Format

- **Opening Statements (30 minutes):** Each panellist will present their thoughts on the designated topics, providing insights into the current state of ESD challenges and future directions. (7 minutes per panellist with a 30-second buffer for transitions).
- **Panel Debate & Discussion (10 minutes):** Panellists will engage in a debate, discussing and potentially challenging or supporting each other's views on the topics presented.
- **Audience Q&A (20 minutes):** The session will conclude with an interactive Q&A segment, allowing the audience to pose questions to the panellists and participate in the discussion.

Expected Outcomes

- Provide a comprehensive overview of the current and future ESD challenges in advanced semiconductor technologies.
- Facilitate a deep discussion on the role of emerging technologies in shaping ESD protection strategies.
- Encourage collaboration between industry and academia to address these challenges effectively.

Keynote & Invited Talks

Dr. Harald Josef Erhard Gossner
Intel Corporation, Germany

Talk Title: ESD Protection Challenges for AI Compute Applications

Abstract: Challenges in ESD protection development have bifurcated into high voltage components and complex, high speed multi die systems using digital leading edge technologies like Gate all around (GAA). Hardware advancements in AI applications rely on heterogenous integration system of chips in downscaled technologies with millions of die-to die interfaces. The roadmap of these technologies is set in context with the available ESD solutions and the need of new developments. The challenges are connected to ESD design concepts, pre-silicon validation and testing. The presentation touches on all of them and indicates the steps to be taken for an ESD protection embedded into these future IC solutions.

Dr. Charvaka Duvvury
iT2 Technologies

Talk Title: Five Decades of ESD Technology Development: Breakthrough Events and Milestones

Abstract: Since the first awareness of its pervasive nature in the electronic industry, beginning during the late 70s ESD development progressed through a series of pioneering papers, which included device physics, the nature of crucial static discharge events, and the evolution of protection concepts driven by the explosion of different IC technologies and circuit design applications. This address will take the audience from the very beginning, highlighting all the key developments from several pioneering researchers. The talk will include the timeline for ESD understanding, ESD testing, ESD control, and ESD protection. Finally, the talk will give a glimpse of what could be important for the next few decades.

Dr. Wolfgang Stadler
Gärtner & Stadler ESD Consulting, Germany

Talk Title: ESD Control for Chip Designers & Test Engineers (*online)

Abstract: ESD control measures, as defined in ESD control standards such as ANSI/ESD S20.20 or IEC 61340-5-1, are crucial for preventing ESD damage to ESD-sensitive items. These ESD control standards require a minimum ESD robustness of 100 V according to HBM and 200 V for CDM for ICs to ensure safe handling. However, the waveforms of actual ESD events in the process do not always match the qualification waveforms, and therefore, passing an ESD qualification does not necessarily guarantee that all handling issues will be avoided. The situation is even more concerning for system-level ESD, such as charged board or cable discharge events, where there is no widely accepted characterization method, and limits in the ESD control standards do not exist. We will discuss the (mis)correlation between IC ESD qualification waveforms and actual risks in handling ICs, boards, and systems, as well as which ESD characterization methods can be used for ESD process assessment.

Keynote & Invited Talks

Dr. Efraim Aharoni
Tower Semiconductor, Israel

Talk Title: Foundry ESD deliverables and characterization for ESD

Abstract: Foundries manufacturing integrated circuits should supply a variety of ESD-related deliverables in their Process Design Kit (PDK). The trade-off between the ESD capability and the signal integrity is reflected in key ESD parameters extracted from dedicated measurements. An effective ESD protection, planned during design level, requires dedicated tools and data exchange. This talk highlights the recommended guidance to the ESD engineer in the foundry, creating and supplying the ESD portion of the PDK and other deliverables. In particular, providing special parameters required for design of an optimized ESD protection in the IC. ESDA Working Group 22 on 'ESD Parameters' technical reports; 'Relevant ESD foundry parameters for seamless ESD design and verification flow' and 'ESD parameters from Intellectual Property (IP) providers', will be highlighted.

Mr. Vinayakam Subramanian
Director, Application Engineering, Ansys, India

Talk Title: 2.5D/3D-IC ESD Reliability Analysis

Abstract: 2.5D/3D-IC have unique ESD challenges due to different IOs, die-to-die links, technologies, suppliers, and design methods that are different from SoC. Managing new ESD risks from die-to-die links considering the effect of different technologies. Handling differences from multiple suppliers of 3D-IC chip structures while adapting different ESD design methods. 3D-IC designers need a systematic and automated way to verify ESD protection on all the chips in 3D-IC to perform ESD analysis all together to overcome all these challenges. Most importantly, to analyze all the chips concurrently, designers need scalable platform to efficiently handle such a large complex designs. This talk provides more details and insight on multi-die ESD analysis to ensure ESD reliability of 3D-IC.

Prof. Nathan Jack
Department Chair, Computer Science and Engineering, Brigham Young University Idaho, USA

Talk Title: Latchup in Contemporary and Emerging CMOS Technologies

Abstract: Latchup remains a critical reliability concern in 7 nm FinFET technologies and beyond. Despite earlier predictions that lower power supply voltages—particularly those near or below 1 V—would eliminate latchup, recent evidence shows that this threat persists. This talk will begin with a concise overview of latchup mechanisms, including single-event latchup (SEL). It will then review key studies from the past 3–5 years addressing latchup risks and mitigation strategies in leading-edge technologies. Finally, the presentation will explore emerging trends such as buried power rails and backside power delivery, with a focus on their implications for SEL susceptibility in future nodes.

Keynote & Invited Talks

Mr. Matthew Hogan
Director of Product Management,
Siemens EDA, USA

Talk Title: Improving the fidelity of ESD margins with context-aware ESD simulation

Abstract: Conservative design rules and constraints are often used in reliability verification flows. By combining the leading solutions for ESD reliability verification and SPICE simulation technologies, SPICE-accurate full-chip simulation becomes possible in a compelling flow for design teams looking to better understand their ESD design margins. We will explore the challenges of traditional parasitic extraction methods, sourcing appropriate SPICE simulation models and demonstrate how a context-aware ESD simulation flow can improve the fidelity of results to better understand ESD design margins, while performing full-chip SPICE-accurate simulations on ESD paths within your design.

Dr. Krzysztof Domanski
Intel,
Germany

Talk Title: ESD codesign in leading-edge Ribbon-FET technologies (*online)

Abstract: The ESD codesign in leading-edge Ribbon-FET or Gate All Around FET (GAA-FET) technologies pose new challenges and opportunities. On the one hand, the ESD design window shrinks permanently with new technology generations with reducing feature-size and victim-breakdown voltages. The Ribbon-FET technology might not offer features traditionally used for ESD codesign like, thyristors, special ESD implantation, drain extensions, or IO devices. A further constraint for ESD design window results from ESD-diodes themselves, because of reduced reverse-breakdown in a dual- diode protection scheme. On the other hand, there are new opportunities arising from Ribbon-FET specific design rules or technology features, that can be turned into advantage for ESD. In this presentation the new trends and techniques for ESD-codesign in Ribbon-FET/GAA-FET will be outlined.

Dr. Steffen Holland
Technical Director,
Nexperia Germany GmbH

Talk Title: System level ESD protection for high-speed data lines

Abstract: ICs with advanced CMOS technology are often used for high-speed data lines. With shrinking structure sizes these ICs become more sensitive to overvoltage during an ESD event. The usage of TVS protection devices enable a high system level ESD protection level but special care must be taken to keep the transient voltage at the IC at an acceptably low level. The presentation will give an overview of the origin of overshoot voltage in TVS protection devices. Device and PCB layout parameters and their effect on the peak voltage at the IC will be shown for a USB-C SuperSpeed data line application.

Keynote & Invited Talks

Prof. Carlo De Santi
Associate Professor,
University of Padova, Italy

Talk Title: TLP effects on normally-off p-GaN gate power HEMTs with Schottky gate

Abstract: In this work, we will present the effect of transmission line pulse tests on normally-off p-GaN gate power HEMTs with Schottky gate metal. The effect of the line charging voltage on both static and dynamic performance will be investigated, as well as the role of the gate bias in the degradation. Deep level characterization techniques will be used to identify the root cause of the degradation and failure processes.

Dr. Akram A Salman
VP/Master Samsung Fondary (ESD team leader)
Samsung Electronics , South Korea

Talk Title: State-of-the-art advances in ESD design and testing for Digital and Analog technologies

Abstract: As the size of digital and analog technologies continues to decrease with each node with added complexity, the challenges associated with developing optimized minimum size ESD solutions have intensified. This is primarily due to the reduction of the ESD design window, the increase in die size, the heightened sensitivity of devices, and the necessity for on-chip system-level ESD protection. In this research, we will delve into the advancements in ESD device and circuit design for state-of-the-art digital technologies, such as FinFET and GAA, as well as analog and HV technologies. Furthermore, we will explore the enhancement of ESD testing methods, including Multi-reflection TLP (MRTLP), to characterize and design more optimal ESD solutions for chip-level and system-level protection. Additionally, we will assess the reverse recovery effects on SOA for high-power devices.

Dr. Ann Concannon
DMTS,
Texas Instruments

Talk Title: Navigating ESD protection challenges in Analog design

Abstract: As the analog semiconductor market continues to expand into diverse applications—ranging from automotive and industrial power management to high-performance RF and sensor interfaces—the challenges of Electrostatic Discharge (ESD) protection become increasingly complex. Unlike digital circuits, where standardized ESD design strategies are well established, analog and mixed-signal ICs demand tailored solutions due to their unique performance constraints, high voltage operation, and sensitivity to parasitic effects. The author will reflect on the key ESD protection options in analog semiconductor design and possible tradeoffs to meet the challenges these present.

Keynote & Invited Talks

Dr. Karuna Nidhi
Manager of ESD-LU and SOA Department,
Tata Semiconductor Manufacturing Pvt. Ltd. (TSMPL), Taiwan

Talk Title: ESD Design flow and Major concern for ICs

Abstract: ESD check flow is an important part of design verification for any integrated circuit (IC) or chip design. To provide sufficient protection against ESD events, IC designers and ESD engineers must make sure that start from the selection of suitable ESD protection devices, its implementation and EDA check must move smoothly to successful Tape-out of the designed product. In this talk, presenter will talk about ESD check flow for IC product design at different phases throughout the product design that will cover together with schematic-based, layout-based flow check along with measurement flow. This approach allows for the avoidance of ESD related design and measurement flaws, reducing the overall design cycle time. Presenter will also highlight on some major concerns during this check flow.

Dr. Slavica Malobabic
ESD Engineer,
Cirrus Logic, Austin, USA

Talk Title: Parasitic PNPs and NPNs in ESD and latch up over different time domains (*online)

Abstract: This tutorial summarizes parasitic NPNs, PNPs, and their interactions within the nano second to milli second time domain. We first go through the basics of Electrostatic Discharge (ESD) and Latch Up (LU). Then we illustrate parasitic NPNs and PNPs during ESD or other transient type events, followed by LU. We will point out issues to watch out for and test structures to mitigate the parasitic NPNs and PNPs for a variety of use cases.

Dr. Ping-Hsun, Su
VP CMOS Technology,
Tata Semiconductor Manufacturing Pvt. Ltd (TSMPL), Taiwan

Talk Title: ESD Challenges from Process transfer into different Fabs

Abstract: As the technology continues to scaling down, the process variation to impact on device and ESD is getting more important. The aggressively scaled feature size leads to serious characteristic degradation and fluctuation of devices. Expect known process variation and randomness effects, there are still many unknown sources of variation that govern uncertainty of devices and ESD circuits. There are more unknown ESD Challenges from process transfer into different Fabs. The author will reflect on the key ESD protection options in semiconductor process , device , and design and possible tradeoffs to meet the challenges these present.

Platform Presentations

Mr. Sadaf Arif Siddiqui
GM-Industry Marketing, Keysight Technologies

Talk Title: Advancements in Semicon test validation with ESD perspective

Abstract: With multiple advancements in the field of Semicon design and manufacturing and with high speed, cutting edge requirements ESD plays a critical role.The talk will highlight some of the latest test methodologies and solutions to handle these complicacies.

Mr. Gopikrishna Siddula
Senior Manager, Mixed Signal IP-IO Design, Western Digital

Talk Title: Designing ESD-Robust ASICs: A Practical Approach for Teams Without ESD Specialists

Abstract: Ensuring ESD robustness in ASICs without an internal ESD expert team demands disciplined design practices and smart use of foundry resources. This presentation outlines practical guidelines for IP and top-level design, focusing on clamp strategies, I/O protection, and cross-domain handling. Key layout techniques such as guard rings and optimized current paths are discussed. EDA-based verification and foundry rule checks are emphasized to meet industry ESD standards and achieve first-pass silicon success.

Prof. Sandip Lashkare
IIT Gandhinagar

Talk Title: Design Challenges and Considerations for Low Voltage System Level ESD Protection Devices

Abstract: Low-voltage (sub-1V) electrostatic discharge (ESD) protection devices are critical for safeguarding low-voltage electronics, including low-voltage GPIO for microcontroller units (MCUs), sub-20nm I/Os, and next-generation interfaces such as USB 3.2 Gen2 and Thunderbolt 4. This talk will provide overview of the low voltage system level ESD protection devices available in the market and discuss the challenges associated in enabling low breakdown voltages for typical Zener/Avalanche diodes. Further, the discussion will cover different physical mechanisms such as punch through, sub-bandgap impact ionization which can be utilized to overcome the low voltage breakdown limitations and design of ESD protection devices using these mechanisms.

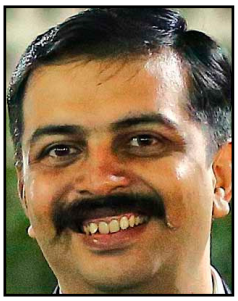
Prof. Laxmeesha Somappa
IIT Bombay

Talk Title: On the ESD requirements and implementation challenges of Neural SoCs

Abstract: Modern Closed-loop Neuromodulation devices help alleviate disease symptoms like epilepsy and Parkinson's tremor using intelligent brain stimulations [1]. Other kinds of neural processors, like phase synchrony processors, rely on deep brain stimulation (DBS) with on-chip rapid phase feature extractions to provide a therapeutic solution for various neurological and psychiatric disorders [2]. With the advent of such devices, the security of the devices becomes an important aspect and is hence associated with power-efficient crypto security engines [3,4]. Such devices are realized as system-onchips (SoCs) with high-density neural (ECoG/AP band) recording analog front-end (AFE), digital backend processors/classifiers [5,6], crypto accelerators and high-voltage compliant programmable neural stimulators. Typically, foundry-provided ESDs are used for the AFE voltage domain (1 V), the digital back-end (<0.7 V) and other associated power management blocks. However, the neural stimulators on the SoC rely on > 10V on-demand generated HV voltage domain in a 65nm CMOS process. This necessitates the need to custom ESD circuits that are implemented in a 65 nm CMOS process to operate beyond 10 V in an on-demand power domain [7,8]. This talk will briefly discuss the challenges associated with the design and implementation of such neural SoCs focusing on ESD design.

1. U. Shin, L. Somappa et al., "A 256-Channel 0.227µJ/class Versatile Brain Activity Classification and ClosedLoop Neuromodulation SoC with 0.004mm2-1.51 µW/channel Fast-Settling Highly Multiplexed Mixed-Signal Front-End," 2022 IEEE International Solid-State Circuits Conference (ISSCC)
2. U. Shin, C. Ding, L. Somappa, V. Woods, A. S. Widge and M. Shoaran, "A 16-Channel 60µW Neural Synchrony Processor for Multi-Mode Phase-Locked Neurostimulation," 2022 IEEE Custom Integrated Circuits Conference (CICC)
3. E. Sarkar, H. Sahu, K. Shaikh and L. Somappa, "On the Implementation of Data Security for Neurostimulation Devices," 2023 IEEE International Symposium on Circuits and Systems (ISCAS)
4. A. Garg, T. Amritkar, S. Vijayakumaran and L. Somappa, "A Cryptographic Security Engine With Sequence Tracker for Implantable Neural Stimulation Devices," 2024 IEEE Biomedical Circuits and Systems Conference (BioCAS)
5. A. P. Sharma, K. A. Rao and L. Somappa, "Hardware Optimization and Implementation of a 16-Channel Neural Tree Classifier for On-Chip Closed-Loop Neuromodulation," in IEEE Transactions on Biomedical Circuits and Systems, vol. 19, no. 2, pp. 244-256, April 2025
6. L. Iyer, A. Bal and L. Somappa, "Calibration-Enhanced 16-Channel On-Chip Seizure Classifier using Gated Recurrent Network," 2025 IEEE International Symposium on Circuits and Systems (ISCAS)
7. T. Das, N. Ahmad, L. Somappa and S. Lashkare, "Enhanced ESD Protection Techniques for 10V Neurostimulator Circuits in 65nm CMOS Technology," 2025 9th IEEE Electron Devices Technology & Manufacturing Conference (EDTM), 2025
8. N. Ahmad, S. Lashkare and L. Somappa, "On the ESD Protection for 10V-Compliant Neural Stimulator in 65nm CMOS Technology," 2025 IEEE International Symposium on Circuits and Systems (ISCAS)

Platform Presentations



Mr. Harshit Dhakad
Principal Engineer,
Intel Technologies India Pvt. Ltd.

Talk Title: Unraveling ESD HBM Failure on a Failsafe Interface in an Advanced FINFET Technology Node

Abstract: This talk provides insights into an HBM failure observed in a product, fabricated using an advance FINFET process node. The failure was detected near the tape-out milestone of the subsequent product stepping. An in-depth analysis of the failure and explores the debugging of the failure through traditional methods, such as Transmission Line Pulse (TLP) measurements is described. A non-conventional approach to modeling of ESD protection, victims to simulate the failure is outlined and the journey towards identifying a viable solution to the ESD failure within the tape-out timeline after considering various trade-offs is described.

Mr. Marcos Hernandez
Senior Staff Scientist,
Thermo Fisher Scientific, USA

Talk Title: Charge Device Model (CDM) Electrostatic Discharge Test Using Low Impedance Contact CDM Method (LI-CCDM)

Abstract: ESD stress in the form of Charge Device Model (CDM) can be challenging for very small devices such as semiconductor dies. The typical Field Induced CDM (FI-CDM) is and air discharge ESD affected by environmental conditions having a profound effect on waveform repeatability, particularly humidity. New methods for testing CDM susceptibility are considered that involved having electrical contact with the pin under test. One of the contact methods considered is Low Impedance Contact CDM or LI-CCDM. This technical talk is a review of how LI-CCDM works, how the data is acquired and what calculations are involved in calculating the peak current. It presents the technical advantages of using LI-CCDM as compared to FI-CDM under certain test conditions.

Mr. Yaddanapudi Vamsi Krishna
Director, ACE Electronics,
Ansys Software Pvt. Ltd.

Talk Title: Simulation Solutions for Electrostatic Discharge

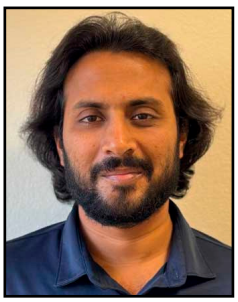
Abstract: Vamsi Krishna has more than 19 years of experience in engineering simulation across Electronics, HVAC and semiconductor industries. Vamsi is in Hyderabad@India. In his current role, Vamsi leads the Ansys India-ASEAN Electronics technical organization and engages with Ansys customers for devising and deploying model-based engineering practices aimed at supporting their digital transformation and “shift-left” journey in product development. Vamsi has significant experience in Chip Package System methodologies and process flow automation. Vamsi hold 4 patents and 1 trade secret in Electronics area and has papers and publications in several reputed conferences and journals. Vamsi has completed his Master’s degree from Indian Institute of Technology, Kanpur.

Platform Presentations

Mr. Tristen Tan
Regional Business Development Manager – Oscilloscopes, ASP Region Rohde & Schwarz

Talk Title: ESD Transient Pulse Verification Based on Oscilloscope

Abstract: This presentation outlines the methodology for verifying Electrostatic Discharge (ESD) transient pulses using oscilloscopes, in accordance with standards. It highlights the importance of high-bandwidth instruments, accurate rise time measurement, and standardized test setups involving ESD simulators and attenuators.



Mr. Surya Viswanathan
ESD engineer,
Infineon Technologies AG, Germany

Talk Title: CDM robustness improvement through decoupling capacitors in advanced CMOS technologies

Abstract: In this presentation, decoupling capacitors as a method of improving the CDM robustness in a 22nm CMOS technology are shown and a quantitative correlation between the capacitance value used and the resulting CDM pass level is derived. vfTLP was used to investigate the physics behind the observed increase in CDM performance which is extendable to other advanced CMOS nodes.

Dr. Shin-ichi Iida
Analytical Solutions Lab Manager,
ULVAC-PHI

Talk Title: Advanced Surface and Interface Characterization for Semiconductor Devices Using XPS and SIMS (*online)

Abstract: X-ray Photoelectron Spectroscopy (XPS) and Secondary Ion Mass Spectrometry (SIMS) are powerful tools for analyzing the composition, chemical states, and depth profiles of semiconductor materials. This presentation highlights practical applications of XPS and SIMS in semiconductor.

Platform Presentations

Mr. Vinod Kumar
Sr. Design Engineering Architect,
Cadence Design Systems

Talk Title: ESD challenges of Designing high-speed interfaces in advanced

Abstract: The advancement systems necessitates high-speed interfaces that require innovative Electrostatic Discharge (ESD) protection schemes. These ESD structures need to be optimized to ensure the fine balancing between required protection and performance of high-speed interface. In this talk the presenter will cover the ESD related challenges for high-speed interface designs in advanced technology nodes.

Ms. Yogendri Vishwakarma
Rambus

Talk Title: Advanced EOS protection techniques

Abstract: Electrical over stress(EOS) is an event which can occur when voltage/current exceeds over the maximum rating of the device for a longer duration of time(ms to s). ESD devices can only handle spikes in voltage/current which occur for a shorter duration of time(in ns or less than us). To address the EOS issue, we need to incorporate regulation loops inside the chip which can protect the I/O and CORE devices while also providing the low resistance clamp paths for the current surges which can happen during the EOS stress condition. In this talk, we address the basic implementation details of EOS and also the challenges associated with it.

Ms. Roopa Hegde
Software Applications Technical Lead Engineer,
Semiverse Solutions

Talk Title: Process window optimization for gate-all-around Electrostatic Discharge (ESD) diode

Abstract: The performance of gated electrostatic discharge (ESD) diode in gate-all-around (GAA) technology is highly sensitive to geometric parameters such as nanowire (NW) cross-sectional area, gate length, and metal contact area. The NW cross-sectional area and gate length are influenced by fabrication process parameters including lithography bias, Si/SiGe etch selectivity, and silicon lateral etch. Additionally, lithography bias and mask misalignment affect the metal contact area. To assess the impact of process variability on ESD diode's architecture, we simulate the gated ESD diode fabrication process. The process window for an acceptable range of geometric parameters was generated by conducting multiple virtual fabrication runs. This study provides insights into the sensitivity of ESD diode's geometry to process variations. SEMulator3D®'s advanced process simulation capabilities enable effective optimization of the process window. This virtual fabrication approach accelerates design iterations, reduces reliance on costly physical prototyping, and enhances reliability by accounting for real-world process variability.

Ph.D. Research Talks

Mayank Yadav (Indian Institute of Science)

Talk Title: Proposal to Achieve the Ultimate Holding Voltage Tunability in Silicon Controlled Rectifiers (SCRs) for a Wide Range of ESD Protection Application.

Abstract: A novel silicon-controlled rectifier (SCR) concept for on chip ESD protection is proposed with holding voltage tunability from as low as 2V to the well breakdown voltage (10V). The novel proposal replaces the standard N+ and P+ implants in N-Tap/Cathode and P-Tap/Anode by P+-N+ implant and N+-P+ implants, respectively. Detailed physical insight of the proposed concept and several derivative concepts is given, explaining the trigger and holding voltage tunability. Besides, additional, rather refined, tunability is depicted by engineering the junction profile of the P+-N+ and N+-P+ implants. The proposed concept together with the junction profile engineering demonstrates the ultimate holding voltage tunability.

Mitesh Goyal (Indian Institute of Science)

Talk Title: Novel Trigger Circuit & SCR Device Co-Engineering Based Local (I/O-VSS & I/O-VDD) ESD Clamp Concepts

Abstract: In this presentation, a novel silicon-controlled rectifier (SCR) based local protection concept will be presented with co-engineered device and trigger circuit. This scheme results in improved latch-up robustness, lower PAD capacitive loading and lower leakage when compared to the reference (state-of-the-art till date) concept. The proposed and reference concepts are realized in Samsung 28nm process for experimental validation and benchmarking. Its TLP/vf-TLP characteristics and other ESD measurement results along with the design trade-offs are presented and compared with the reference concept. A TCAD based device and circuit co-optimization (DTCO) methodology is also presented. The proposed concept can realize the demanding I/O needs of SCR based local clamps, qualified for HBM to CDM time domains, and meeting ESD specs required for high speed I/O buffers.

Harsh Raj (Indian Institute of Science)

Talk Title: Dynamic Breakdown Voltage and Overvoltage Margin in beta-Ga2O3 based devices

Abstract: In this presentation, we report transient breakdown voltage of on-wafer β-Ga2O3 Schottky barrier diodes (SBDs) in ultra-short (sub-μs duration) pulses based on an electrostatic discharge system setup. β-Ga2O3 SBDs show a dynamic breakdown of 800 V in 10 ns pulse excitations, twice that of the static breakdown. Additionally, the device can withstand overvoltage pulse stresses for varying number of switching cycles at pulse durations below 100 ns. Detailed experimental analysis reveals the role of trap states and trapping-induced temporal and spatial field evolution in the observed device behavior. A clear understanding of the device degradation mechanism in these overvoltage stresses is needed for design of devices with improved reliability under rapid switching events that they may be subjected to in power electronic circuits.

Adaptive Self-Healing ESD Protection for IoT Using AI-Driven Dynamic Voltage Clamping

Mudit Kumar Singh (Department of Electronic Science, University of Delhi)

Abstract: This work introduces a novel AI-reconfigurable ESD protection circuit for IoT systems. Combining GaN TVS arrays with tunable MIM capacitors, the design dynamically adapts clamping topology in real-time using embedded machine learning (ML). The ML classifier predicts surge profiles (<100 ns) to optimize protection during oscillating discharges, reducing residual voltage by 40% vs. static solutions. Validated via SPICE and TLP testing, the system achieves 30 kV IEC 61000-4-2 robustness with 50% smaller footprint and 30% lower BOM cost. Applications include wearables, medical sensors, and industrial IoT where size and adaptive reliability are critical.

From Gate to Ground: A Beginner's View into On-Chip ESD DesignFrom Gate to Ground: A Beginner's View into On-Chip ESD Design

Nisarga D K (Tapeout engineer)

Abstract: Electrostatic Discharge (ESD) is one of the major causes of chip failure in modern VLSI systems. As devices shrink and voltages decrease, even small electrostatic charges can damage sensitive transistors. This poster presents a beginner-level overview of ESD and common on-chip protection techniques such as diode clamps and gate-grounded NMOS (GGNMOS). The aim is to highlight how ESD protection is integrated into the design flow and why it is critical during chip handling, testing, and packaging. Simple block diagrams and real-world examples will be used to explain the concepts clearly. This work is intended for students and new professionals looking to understand the basics of ESD-safe design in semiconductor devices.Electrostatic Discharge (ESD) is one of the major causes of chip failure in modern VLSI systems. As devices shrink and voltages decrease, even small electrostatic charges can damage sensitive transistors. This poster presents a beginner-level overview of ESD and common on-chip protection techniques such as diode clamps and gate-grounded NMOS (GGNMOS). The aim is to highlight how ESD protection is integrated into the design flow and why it is critical during chip handling, testing, and packaging. Simple block diagrams and real-world examples will be used to explain the concepts clearly. This work is intended for students and new professionals looking to understand the basics of ESD-safe design in semiconductor devices.

Structural Innovations for ESD Protection in BSPDN: Backside Ground Sink Layer and Dual-Layer TSV Isolation

P R Teja Sree (Graduate Student)

Abstract: As Backside Power Delivery Networks (BSPDN) emerge in advanced 3D IC packaging, new ESD vulnerabilities surface due to high-density TSVs and exposed backside pads. This poster proposes two novel strategies to enhance ESD resilience (1) a Backside Ground Sink Layer (BGSL): a dedicated, low-resistance grounding plane beneath the BSPDN to instantly absorb discharge and redirect current away from logic paths, and (2) Dual-Layer TSV Isolation (DLTI): a reengineered TSV structure with an isolating shell to contain ESD within the core and prevent cross-talk. Together, these techniques offer a scalable, layout-friendly approach for next-generation chip stacking under extreme performance demands.

System-Level ESD Resilience with Verilog and Adaptive Filtering

Ambika (BMS College of Engineering)

Abstract: This system-level approach integrates Verilog-A device models with Xilinx Vivado-based fault injection to simulate ESD resilience in digital architectures. It abstracts electrostatic discharge effects into programmable test vectors (IEC 61000-4-2 compliant) while employing adaptive median filtering with dynamic window sizing (3×3 to 5×5) for noise mitigation. The framework enables co-simulation of analog ESD transients (via Spice) and digital signal integrity verification (BRAM/CRC checks), achieving 5× faster validation cycles than physical testing. Validated on medical ECG systems, it reduces phase errors by 98% in 28nm FDSOI nodes. While quasi-static modeling limits full electrothermal analysis, the workflow supports ISO 26262 ASIL-D compliance, making it ideal for automotive/medical ICs requiring <10% signal distortion under 150MHz clock domains.

Compact ESD Protection Strategies for IoT Edge Devices

Srinidhi Shetty (DSCE,Bangalore)

Abstract: With the increasing deployment of IoT edge devices in uncontrolled environments, robust yet compact ESD protection becomes critical. GGNMOS and diode-based ESD clamps optimized for low-power and area-constrained applications. Emphasis will be on understanding trade-offs in clamping voltage, leakage current, and layout impact. Simulation-based evaluation methods will be proposed to assess the performance of basic ESD topologies. This work aims to offer a learning-oriented framework for beginners in chip design to understand real-world reliability challenges in ASIC development.

Safeguarding IC Integrity: Runtime-Efficient Detection of ESD Devices Misuse with Calibre PERC

Kunwar Tarun, Kislaya Sharma, Ertugrul Demircan (NXP India Private Limited, Noida, India)

Abstract: Unintended deployment of ESD protection devices in non-ESD circuitry introduces critical risks, including elevated leakage currents, timing degradation, absence of aging models, and susceptibility to latch-up. Despite functional correctness, such violations degrade area efficiency, yield, and long-term reliability. This work presents a robust methodology leveraging Calibre PERC to detect misplaced ESD devices at both schematic and layout levels. The approach integrates rule-based checks and hierarchical analysis to optimize runtime and detection accuracy. Early identification enables pre-silicon resolution of ESD misuse, ensuring design robustness and compliance with reliability constraints across advanced process nodes and complex mixed-signal design environments.

Custom ESD Protection for 10V-Compliant Neural Stimulator in 65nm CMOS Technology

Tanay Das, Naef Ahmad, Sandip Lashkare, Laxmeesha Somappa (IIT Gandhinagar, IIT Bombay)

Abstract: Implantable neural circuits have broad applications, such as treating neurological disorders. To ensure reliability against electrostatic discharge (ESD) damage during fabrication, packaging, or handling, robust ESD protection is essential. A fully integrated, closed-loop neuromodulation SoC, featuring on-site recording, digital processor, and a high-voltage compliant stimulator, constrained by cost, is implemented in 65 nm CMOS technology. Custom ESD protection is needed, as foundry-provided solutions cannot withstand the high voltages required for reliable current stimulation. This work introduces a ±10V compliant stimulator with integrated custom on-chip ESD protection in a 65 nm process, validated for the HBM model via post-layout TLP simulations.

Asymmetric NIPIN Diode for Low-Voltage, Low-Capacitance Unidirectional ESD Protection.

Navin Maheshwari, Krish Patel, Kshitij Agarwal, Hasan Ali, Ritesh Kumar, Sandip Lashkare
(Indian Institute of Technology, Gandhinagar)

Abstract: Ultra-low-voltage TVS diode is critical for the protection of low-voltage electronics such as Sub 20 nm I/Os, next-gen USB, Thunderbolt etc. Existing system level solutions rely on pn diodes operating in Zener breakdown, limited by the bandgap, and even advanced designs such as punch through or gradedbase diodes the voltage is ~1V. Here, we propose a triangular barrier silicon NIPIN diode, achieving breakdown from 0.5V up to 3V utilizing sub-bandgap impact ionization. Further, symmetry control is shown by adjusting intrinsic region lengths and dopings. Compared to existing devices, it offers nearideal standoff and clamping voltages - marking a major advancement for low-voltage electronics.

Predictive TCAD-Based Design of Customized ESD Protection with Low Clamping Voltage for 10V Neurostimulator Circuits in 65nm CMOS Technology

Navin Maheshwari, Laxmeesha Somappa, Sandip Lashkare
(Indian Institute of Technology, Gandhinagar & Indian Institute of Technology, Bombay)

Abstract: Effective Electrostatic Discharge (ESD) protection is critical for 10V neurostimulator circuits in 65nm CMOS, where strict area and voltage constraints limit design choices. Standard diodes fail to meet breakdown voltage (>10V), clamping voltage (<16V), and dynamic resistance (<6Ω). This work presents a TCAD-based Back-to-Back diode ESD protection design. Doping profiles and junction spacing are optimized to match target breakdown and dynamic resistance while minimizing current crowding. The layout, with n-diode centrally positioned and p-diode surrounding it, ensures balanced current flow and reduced thermal hotspots. The final design achieves clamping &th;16V, 10× lower resistance, and area-efficient robust ESD protection.

Physical insights into ultra-low capacitance transient voltage suppression diode for system level ESD protection

G.Yashan Kumar , N. Maheshwari, Sandip Lashkare (IIT Gandhinagar)

Abstract: To maintain signal integrity, low capacitance ESD protection is essential for the applications having high-speed data interfaces such as HDMI, USB etc. Typical Zener diodes offer good ESD protection, but increasing their area also increases capacitance. Ultra-low-capacitance TVS (ULC-TVS) diode is one of family TVS diodes which provides lower capacitance than standard TVS diodes. This work provides in depth physical insights into how fabrication aspects(geometry, doping profiles, finger structures, trench design) impact ULC-TVS ESD performance. It also proposes a design strategy that improves ESD protection while keeping low capacitance and reducing area usage compared to conventional Zener diodes.

ESD Challenges in 2nm & Beyond: Providing Innovative Solution for Next-Gen Memory and Logic Devices

Archisman Banerjee (Student , Kalinga Institute Of Industrial Technology)

Abstract: Electrostatic Discharge (ESD) offers significant reliability constraints in advanced logic and memory devices. In the current era of 2nm technology , architectures like MRAM , 3D- NAND are highly vulnerable to ESD. The major ESD failure processes like interconnect damage , gate oxide breakdown and their solutions need to be addressed. This study highlights innovative strategies like advanced SCR structures and artificial intelligence based optimized designs. The findings focuses on maintaining a balance between device strength , overhead area and processing speed , thus ensuring proper and robust device design.

IO integration rule to streamline the early PERC signoff at SoC level

Annu Kumari (Synopsys)

Abstract: PERC signoff is crucial for reliability checks of ESD/Latch-up to provide the final SoC signoff. SoC architecture has diverse interface IPs, including IOs, which are more prone to ESD/latch-up risk. Nowadays, industries are looking for SoCs which are validated with PERC tools. PERC validation at SoC is complex, since thousands of PERC rules, high run-time, and late catching of PERC violations causing delays in signoff. In this poster, we exhibit PERC analysis done during the IP development such that SoC designers only need to maintain the IO Integration-rule and robust connectivity between Bump to Signal/power/ground pad for early PERC signoff.

IRC- IO RING COMPILER

Priyanshi Jain, Praveen Jakki, Avinash Gupta, Anurag Mittal (Synopsys)

Abstract: IO Ring is a key factor for any SoC Design and Building the same manually is a challenging task. Designer also need validate the IO ring for all the ESD Integration rules. The proposed IO Ring Compiler tool establishes the automated IO RING, incorporating necessary cells and adhering integration rules with inbuilt validation. It also validates any pre-built IO ring DEF. The advantages are robust and flawless IO ring development, reduced cycle time and increased Productivity. The proposed utility has been verified across multiple technology nodes and is in use for all IO RING REVIEW queries received through Customers.

ESD Challenges in 2nm & Beyond : Providing Innovative Solution for Next-Gen Memory and Logic Devices

Sunilkumar (Globalfoundries)

Abstract: eFUSE technology, widely adopted as a One-Time Programmable (OTP) memory solution, plays a critical role in security-centric applications across various process nodes. Beyond its security applications, eFUSE is instrumental in enabling redundancy, chip self-repair, and reconfiguration—both at the factory and in-field thereby enhancing overall chip yield[1]. These capabilities are significantly augmented through integration with advanced Built-In Self-Test (BIST) and Built-In Self-Repair (BISR) methodologies[2].

From an implementation standpoint, the long-term reliability of electrical fuses is paramount to ensuring sustained chip functionality. Consequently, robust Electrostatic Discharge (ESD) protection becomes essential in eFUSE design. This poster presents a detailed case study addressing the system-level verification challenges encountered during the development of ESD protection for eFUSE IP in 55BCDlite technology. Key focus areas include technology compatibility, drive strength optimization, and compliance with Human Body Model (HBM) and Charged Device Model (CDM) test requirements. The study also outlines ESD pass/fail criteria at the subsystem level, offering insights into the design and verification strategies necessary for reliable eFUSE deployment in mixed-signal and high-voltage environments.

[1] W. Tonti et al., “Product Specific Sub-Micron E-Fuse Reliability and Design Qualification” IRPS Proceedings, p161 (2004)
[2] https://www.design-reuse.com/article/61534-optimal-otp-for-advanced-node-and-emerging applications D&R Industry Articles

IO integration rule to streamline the early PERC signoff at SoC level

Annu Kumari, Avinash Gupta, Anurag Mittal (Synopsys)

Abstract: PERC signoff is crucial for reliability checks of ESD/Latch-up to provide the final SoC signoff. SoC architecture has diverse interface IPs, including IOs, which are more prone to ESD/latch-up risk. Nowadays, industries are looking for SoCs which are validated with PERC tools. PERC validation at SoC is complex, since thousands of PERC rules, high run-time, and late catching of PERC violations causing delays in signoff. In this poster, we exhibit PERC analysis done during the IP development such that SoC designers only need to maintain the IO Integration-rule and robust connectivity between Bump to Signal/power/ground pad for early PERC signoff.

ESD CDM Target Management using Optimized I/O

Hemant Ahire, Bhawana Adhikari, Siddharth Singh, Anurag Mittal (Synopsys)

Abstract: Most of the foundry provides different ESD diodes, supply clamps depending on CDM target current i.e. 5A, 7A, 10A etc. For lower techno nodes higher CDM current target requires very big ESD components sizes which consumes significant area and leakage budget of a SOC. In this poster we present how we can use same optimized I/O across all CDM targets. We have developed few solutions during I/O ring implementation i.e. by varying distance rules, split clamps etc.

Electrifying Reliability: Fast-Track ESD Validation for Next-Gen Medical & Automotive Chips

Ambika (BMS College of Engineering)

Abstract: This system-level approach integrates Verilog-A device models with Xilinx Vivado-based fault injection to simulate ESD resilience in digital architectures. It abstracts electrostatic discharge effects into programmable test vectors (IEC 61000-4-2 compliant) while employing adaptive median filtering with dynamic window sizing (3×3 to 5×5) for noise mitigation. The framework enables co-simulation of analog ESD transients (via Spice) and digital signal integrity verification (BRAM/CRC checks), achieving 5× faster validation cycles than physical testing. Validated on medical ECG systems, it reduces phase errors by 98% in 28nm FDSOI nodes. While quasi-static modeling limits full electrothermal analysis, the workflow supports ISO 26262 ASIL-D compliance, making it ideal for automotive/medical ICs requiring <10% signal distortion under 150MHz clock domains.

TCAD modeling of STI diode response to ultrafast ESD event during D2D and D2W bonding process

Emanuele Groppo[1,2] , Harshit Dhakad[3], Harald Gossner[1], Anand Sharma[3]
([1]Intel Deutschland GmbH, [2]Technische Universität München, [3]Intel Technologies Inida Pvt. Ltd)

Abstract: Charged Device Model (CDM) events can occur during the bonding process in 2.5D or 3D technologies. Simulations and measurements show that such CDM events are characterized by ultrafast rise times (few tens of picoseconds) and peak current pulses that can reach several hundreds of milliamperes. In such conditions, diode forward recovery effect causes voltage overshoots that can lower the failure level of thin gate oxide (GOX) victims. TCAD simulations show that voltage overshoots increase with faster rise time pulses, posing a severe reliability threat for tightly constrained ESD protection of Die-to-Die (D2D) and Die-to-Wafer (D2W) interfaces. To ensure realistic simulation results, a voltage-driven simulation setup is proposed replacing the commonly used current-driven one. Diode transient response becomes the main concern for ESD protection of such interfaces to comply with GOX safe operating limits.

Method of ESD characterization and modeling of ESD networkfor CDM predictive simulation

Nicolas Richaud,Nicolas Richaud, Ritesh Agarwal, Harshit Dhakad, Harald Gossner, Florian Klotz, Umair Ishfaq, Robert Haeussler, Krzysztof Domanski, Anand Sharma (Intel)

Abstract: This poster presents a methodology for electrostatic discharge (ESD) characterization and modeling of ESD victims experiencing fast voltage overshoots under Charged Device Model (CDM) conditions. Dedicated test structures were developed to accurately characterize overshoot effects using an ultrafast Transmission Line Pulse (UFTLP) setup with current pulse rise times (>20 picoseconds). The diode model was adjusted to reflect forward recovery behavior during the rapid rise times of CDM current. Additionally, a testbench for predictive CDM simulations is proposed, enhancing the reliability of ESD protection strategies by accurately simulating the fast transient responses of ESD victims.

Performance projection of Junction-less CFET

Ayaz Mumtaz Ansari (Jamia Millia Islamia)

Abstract: In this work, we present the device-level modeling and comparative performance analysis of a 2D Complementary Field-Effect Transistor (CFET) and its Junctionless counterpart (JL-CFET) using Synopsys Sentaurus TCAD. The electrical behavior of both devices is evaluated through extraction of NMOS and PMOS transfer characteristics, voltage transfer characteristics (VTC), and transient response curves. Furthermore, we investigate the influence of gate metal work function (WF) variation on the performance of both NMOS and PMOS configurations, and identify optimized WF values for the JL-CFET structure to enhance its performance. To complement the TCAD-based study, a predictive machine learning model is developed that estimates the transfer characteristics of JL-CFET devices for a given WF input. The proposed integration of TCAD simulations with AI-based prediction offers a powerful approach for accelerating device optimization in future CMOS technologies.

Self-Contained Lattice-Ag Filament Analog Switching in $AgHfO_{3-x}$ Memristors Enabling Stable Synaptic Behavior and Associative Learning

Swaraj Mukherjee (IIT Jodhpur)

Abstract: Silver-doped perovskite $AgHfO_{3-x}$ naturally generates uniform hybrid conduction paths of lattice Ag and oxygen vacancies, removing the need for external active electrodes and preventing random filament formation typical of HfO_2 devices. Introducing extra oxygen during deposition reduces vacancy density, boosting switching stability and ON/OFF contrast. The Au/$AgHfO_{3-x}$/FTO memristor delivers stable analog resistive switching, emulates key synaptic behaviors potentiation, depression, paired-pulse facilitation and supports associative learning via a Pavlovian conditioning protocol. CMOS compatibility and combined memory neuromorphic performance make $AgHfO_{3-x}$ memristors a scalable hardware platform for brain-inspired computing.

$CuGa_2O_4$ based Memristor device for Synaptic Plasticity and Associative Learning

Ayan Chatterjee (IIT Jodhpur)

Abstract: We illustrate a spinel $CuGa_2O_4$-based memristor showing stable bipolar resistive switching under low voltage operation and with good endurance, which is a prime contender for future memory devices. Besides digital memory, the device exhibits analog behavior allowing synaptic plasticity such as paired-pulse facilitation, potentiation/depression, and conversion from short-term to long-term plasticity. Importantly, it replicates associative learning based on Pavlovian conditioning. These characteristics identify the two-fold potential of $CuGa_2O_4$ memristors for both neuromorphic and non-volatile memory purposes, making them strong contenders to realize brain-inspired hardware systems.

Formation Mechanism and Spectroscopic Characterization of ZnO Layers Buried in Si/ZnO/HfO_2 Heterostructure

Jay Sharma (Saha Institute of Nuclear Physics)

Abstract: Metal oxides are vital for optoelectronic, piezoelectric, and magnetic applications. This study demonstrates the controlled synthesis of zinc oxide (ZnO) thin films on n-type silicon via internal oxidation of a buried zinc (Zn) layer beneath hafnium dioxide (HfO_2). X-ray diffraction confirmed the full conversion of Zn into a ZnO/HfOx heterostructure. Low-temperature photoluminescence at 4 K showed sharp near-band-edge emissions at ~3.37 eV, indicating high optical quality. These findings highlight a viable route to fabricate buried wide-bandgap oxide heterostructures, offering potential for advanced electronic and photonic device integration across a variety of emerging technologies.

DIRECT: Enabling Scalable Processing-In-Memory via DPU-to-DPU Communication

Prateek P Kulkarni (PES University)

Abstract: The exponential growth in dataset sizes and model complexity has made distributed training a necessity for modern machine learning (ML) workloads. However, conventional processor-centric architectures struggle with the data movement bottleneck, leading to suboptimal performance and energy efficiency. Processing-In-Memory (PIM) has emerged as a promising solution, but current PIM systems face critical scalability challenges due to mandatory host CPU mediation for inter-DPU communication. We present DIRECT, a novel architecture enabling CPU-free DPU-to-DPU communication through a hierarchical crossbar network with hardware-level synchronization primitives. Our key innovations include: (1) Atomic Gradient Accumulation Units (AGAUs) for efficient local parameter updates, (2) a Distributed Synchronization Controller (DSC) for global coordination, and (3) locality-aware training algorithms. Comprehensive evaluations on industry-standard ML workloads demonstrate a 2.9× speedup in training time, 65% reduction in energy consumption, and 92% parallel efficiency at 2048 DPUs (vs. 25% baseline), all with minimal hardware overhead (0.51mm² area, 205mW power in 28nm process). DIRECT outperforms state-of-the-art PIM systems and bridges the gap with specialized GPU accelerators for distributed ML training, paving the way for more energy-efficient and scalable ML infrastructures.

Enhanced ESD Reliability of AlGaN/GaN MIS-HEMTs Using a p-Type Oxide Passivation

Mohammad Ateeb Munshi (Indian Institute of Science)

Abstract: This work presents a novel device-level solution to enhance ESD reliability of AlGaN/GaN MIS-HEMTs using a p-type AlTiO-based passivation. Extensive ESD testing, including TLP and VF-TLP under various stress conditions, shows that AlTiO significantly outperforms conventional SiN passivation. It suppresses channel electric field peaks, reducing self-heating and eliminating thermoelastic strain, thus improving off-state and semi-on-state ESD performance. Enhanced robustness is also observed under floating gate and gate–source stress. Raman, thermoreflectance, EL, and FE-SEM analyses reveal reduced thermal and impact ionization failures, validating AlTiO's effectiveness in improving ESD resilience and uncovering associated failure mechanisms.

Comparative study for optimum placement of substrate trigger points in STI bound SCR

Mukesh Chaturvedi (Samsung Semiconductor India Research)

Abstract: To bring down the trigger voltage (Vt1) of a STI bound SCR within ESD design window, we need to inject charges into the substrates to enable the high base current needed for early turn on of the parasitic PNP or NPN transistors. The placement of this injection point is closely related to the effect of injected charges on trigger voltage (Vt1), Holding voltage (Vh) and Triggering time. Hence position of trigger point is strategic in design of SCR. We present comparative study of various locations of trigger points in this poster.

TCAD Calibration Methodology for Accurate ESD Simulation

Mitesh Goyal, Mahesh Vaidya, Mukesh Chaturvedi, Mayank Shrivastava (Indian Institute of Science)

Abstract: For accurate ESD simulation device architecture and its operational physics impacts the overall behavior of the device. This demands good calibration of the TCAD environment with the physical process. The triggering mechanism of most of the ESD protection device is driven by an avalanche breakdown event, which triggers in the critical electric field within the device. The field distribution has a major dependency on the doping profile of the device. And therefore, it is highly recommended to have a calibrated doping profile in TCAD simulations.

In this poster, we are presenting how to simulate the ESD devices (for example: SCR) with a calibrated TCAD environment. The calibration starts with obtaining the actual doping profiles for the TCAD simulation, where we use PDK (Process Design Kit) data as an input. In order to capture the N+/P+ profile; we use the same cross-section of diffusion resistor as the PDK layout with various lengths. The different values of the diffusion resistor's IV-characteristics have been extracted with a circuit simulator and can be used as an input to TCAD. While simulating the diffusion resistor in TCAD the related physics has been invoked, which helps the TCAD to capture all the important physics in order to replicate the accurate IV-behavior. The matching of TCAD and PDK simulated characteristics of diffusion resistors has provided us with the doping profile for N+/P+ taping. The same procedure has been followed with the N-Well and P-Well resistor in order to get the N-Well/P-Well doping profile. This calibrated N+/P+ doping profile along with N/P-Well doping profile has been further used to create P+/N-Well Diode and N+/P-Well diode for further validation. Furthermore, all these calibrated profiles have been used in order to calibrate MOSFET in order to capture a little more information about the device gates. The MOS-Capacitance and MOSFET IV characteristic from the PDK has been used in TCAD to extract more information like; Vt Implant profile, Halo Implant profile, oxide thickness and so on.

The calibrated doping profiles extracted through TCAD simulations, are then used to create the digital twin of SCR. As in the ESD simulation, where the high voltage and high current injection event happens, requires a very precise calibration environment in terms of physics declaration also. The charge transport models like Doping, Electric Field and Temperature dependent models have been invoked during the simulation. Moreover, to capture the device temperature role ESD simulation accurate thermal boundary condition has been used along with the thermal resistance component. This is very essential to capture the instability which occurs when a device triggers from off-state to on-state.

By following this procedure and techniques, we were able to perfectly match the ESD parameters like Trigger Voltage, Trigger Current, Holding Voltage, Holding Current, Failure Current, etc. Along with this, the real-time transient oscillations have also been captured during the transition of the device from trigger to holding point, which happens due to the moving filament event.

Improving the latch up robustness of SCR by Injection terminal engineering

Jigyasa Shrivastava (Indian Institute of Science)

Abstract: Substrate Triggering is one of the most popular method to bring the trigger voltage of SCR in ESD safe window of operation. But the placement of this current injection point for SCR trigger impacts its latchup susceptibility. In this poster, an state of the art STI bounded SCR with trigger circuit is implemented in a bulk planar technology and many variations of current injection point is implemented to test the latch up robustness of the devices. We observe that though ESD characteristics are better for certain geometrical variations, but they come at the cost of lower latch-up robustness.

Missing Trigger Circuit Action and Device Engineering for Conventional Nanoscale SCR

Mitesh Goyal, Mukesh Chaturvedi, Mahesh Vaidya, Mayank Shrivastava (Indian Institute of Science)

Abstract: In this work co-optimization of silicon-controlled rectifier (SCR) ESD characteristics with its low voltage trigger circuit is presented. Resistance and Capacitance (RC) controlled thick gate NMOS and PMOS based circuits have been explored and compared. The design approach is discussed and presented for low trigger SCR for two different trigger circuits. In the process we find that some of the trigger circuits previously reported in literature do not work as desired until co-optimized device engineering techniques are used. The circuit insights are explored using well calibrated electrothermal 3D process and device TCAD mixed mode simulations.

Small Signal Assisted Monitoring of Channel in TMD FETs

Utpreksh Patbhaje (Indian Institute of Science)

Abstract: We propose a small signal analysis methodology which is capable of monitoring TMD channel health in FETs and can be used to evaluate WF changes in TMD devices providing a quick way to assess stress history of the TMD channel. The evolution of small signal impedances of pristine device till breakdown under ON, OFF, and Open gate conditions are analyzed using C-f and C-V sweeps. Incremental stressing field across source-drain reveals a metallic nature of channel encountered well before catastrophic breakdown. This methodology can be used to define safe operational regimes for the TMD FETs.

Inconsistencies in current Trends in MoSe2 FETs Under Long Term Operation

Megha Yadav (Indian Institute of Science)

Abstract: TMDs like $MoSe_2$ are promising materials for future electronics, but realizing both NMOS and PMOS functionality remains challenging. This study investigates the conduction behavior of Pd-contacted $MoSe_2$ FETs under back-gated vacuum operation. After applying lateral fields, we observed enhanced n-type and degraded p-type currents, linked to strain-induced effects. The results show a 25% increase in n-type and 300% decrease in p-type conduction. Strain, arising even under low fields, impacts ambipolar devices due to inverse piezoelectric effects. This emphasizes that in order to guarantee stable n- and p-type operation, strain-induced inverse piezoelectric effects must be addressed in future 2D device frameworks.

Charge Neutrality Point Alignment Strategy using Terminal Voltages in MoSe2- FETs

Raising Archana Bairiganjan Mohapatra (Indian Institute of Science)

Abstract: 2D materials like $MoSe_2$ hold promise for next-generation electronics due to features such as ambipolarity and tunable charge neutrality. However, intrinsic n-type behavior and Fermi-level pinning at contacts limit their effectiveness in sensing applications. We present a charge neutrality point (CNP) alignment strategy using terminal voltages in $MoSe_2$ FETs, where Pd-contacted back-gated devices exhibit tunable ambipolarity. By keeping a constant VSD = 1 V/μm and varying drain offset (−15 V to +30 V), we shift the threshold voltage from −12 V to +18 V and control VCNP. This electrostatic modulation enables resistance tuning from 21 MΩ to 0.24 MΩ. Such deterministic control over the CNP is pivotal for applications in photodetectors, chemical sensors, and analog amplifiers, where accurate modulation of current around the threshold voltage is essential for optimal performance

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